Amendment to Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method of creating a design for a semiconductor memory and an associated memory cell array, comprising:

a. providing a leaf cell design for use by a memory compiler for a semiconductor memory, the leaf cell design further comprising a power management circuit design as a leaf cell for a memory ~~circuit,~~ circuit and a control supply voltage;

b. acquiring a user input describing a parameter of a circuit, the circuit to comprise the leaf cell design;

c. providing a user-selectable option to selectively allow enablement of an ultra low power feature; and

d. creating a semiconductor memory design by the memory compiler which incorporates the power management circuit in a compiled semiconductor memory macro when the user-selectable option is enabled

wherein the control supply voltage includes a netlist identifier which is unique with respect to a netlist identifier for a control supply voltage of the memory cell array.

2. (Original) The method of claim 1, wherein the memory compiler is adapted to create a design for at least one of (1) a static random access memory, (ii) a read only memory, (iii) an embedded flash memory, or (iv) a single transistor random access memory.

3. (Original) The method of claim 1, wherein the power management circuit design is adapted to reduce leakage power resulting from a circuit resulting from use of the memory compiler.

4. (Currently Amended) The method of claim 1, wherein the power management circuit design ~~is adapted to provide~~ further comprising a first control voltage power supply ~~adapted to provide~~ for providing power to a circuit peripheral ~~to a memory cell array~~ and ~~to provide~~ a second control voltage power supply ~~adapted to provide~~ for providing power to the memory cell array.

5. (Original) The method of claim 4, wherein the power management circuit design comprises:

a. a first control supply voltage design, adapted to produce the first control voltage power supply; and

b. a second control supply voltage design, adapted to produce the second control voltage power supply;

c. wherein the second control voltage power supply is a separate voltage supply with respect to the first control voltage power supply.

6. (Previously Presented) A method of creating a design for a semiconductor memory, comprising:

a. providing a leaf cell design for use by a memory compiler for a semiconductor memory, the leaf cell design further comprising a power management circuit design as a leaf cell for a memory circuit;

b. acquiring a user input describing a parameter of a circuit, the circuit to comprise the leaf cell design;

c. providing a user-selectable option to selectively allow enablement of an ultra low power feature; and

d. creating a semiconductor memory design by the memory compiler which incorporates the power management circuit in a compiled semiconductor memory macro when the user-selectable option is enabled

wherein the power management circuit design is adapted to provide a first control voltage power supply adapted to provide power to a circuit peripheral to a memory cell array and to provide a second control voltage power supply adapted to provide power to the memory cell array providing the control supply voltage of the memory periphery circuit with a netlist identifier which is unique with respect to a netlist identifier for the control supply voltage of the memory cell,

wherein the power management circuit design comprises:

(i) a first control supply voltage design, adapted to produce the first control voltage power supply; and

(ii) a second control supply voltage design, adapted to produce the second control voltage power supply;

(iii) wherein the second control voltage power supply is a separate voltage supply with respect to the first control voltage power supply.

7. (Original) The method of claim 5, wherein the first control voltage power supply further comprises:

a. a voltage supply; and

b. a control signal.

8. (Previously Presented) The method of claim 7, wherein the voltage supply is a variable voltage supply to provide a substantially zero voltage.

9. (Original) The method of claim 5, wherein the second control voltage supply is a variable voltage supply, further comprising:

a. allowing the second control voltage supply to operate in a minimum voltage level capable of sustaining data in the memory cell; and

b. allowing the second control voltage supply to have a substantially zero voltage in a static mode.

10. (Cancelled.)

11. (Original) An electronic circuit created using the process of claim 1.